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EXAMINER

TSAI, HENRY

ART UNIT	PAPER NUMBER
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2181

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/039,579	<b>Applicant(s)</b> RODGERS ET AL.	
	<b>Examiner</b> Henry W.H. Tsai	<b>Art Unit</b> 2181	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12/01/05.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 70-76 and 78-115 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 98-115 is/are allowed.
- 6) ☒ Claim(s) 70-76 and 78-97 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12/01/05 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/01/05</u> | 6) <input type="checkbox"/> Other: _____  |

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**DETAILED ACTION**

***Drawings***

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "792" and "795" (page 23); and "1100" (page 27). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

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***Claim Objections***

2. Claim 78 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Note claim 78 should not depend from the cancelled claim 77.

***Claim Rejections - 35 USC § 112***

3. Claims 89-92 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 89, lines 1-2, "said plurality of partitionable resources" lacks proper antecedent basis since it was not defined.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

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***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 70-76, and 78-97 are rejected under 35 U.S.C. 102(e) as being anticipated by Emer et al. (U.S. Patent No. 6,493,741) herein referred to as Emer et al.'741.

Referring to claim 70, Emer et al.'741 discloses as claimed, a processor (CPU 100 see Fig. 2) comprising: a plurality of execution units (thread processing units TPU #1 to TPU #N see Fig. 2) to execute a plurality of threads; suspend logic (certainly inside the Emer et al.'741's system, such as a control unit, see Fig. 2) to set a monitor address (lock address 139 in memory 137, see Fig. 2) in response to a first instruction (such as LDQ ARM R1, (R5), see Col. 6, line 56) in a first thread according to an implicit operand in a predetermined

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register (event identification register 103, see Figs. 2 and 7) and to suspend the first thread in response to a second instruction (such as QUIESCE instruction, see Col. 6, lines 55-59) of the first thread; a monitor (event monitor 109, see Fig. 2) to cause resumption (see Col. 6, lines 1-6 regarding the TPU resumes execution) of the first thread in response to a memory access (see Col. 6, lines 1-6, regarding a change to the lock 139 referenced in the event identification register 103) to the monitor address.

Referring to claim 93, Emer et al.'741 discloses as claimed, a processor (CPU 100 comprising thread processing units TPU #1 to TPU #N see Fig. 2) comprising: a front end (comprising fetch thread chooser 301, see Fig. 3 or map thread chooser 351, see Fig. 4) to receive a first instruction (such as LDQ ARM R1, (R5), see Col. 6, line 56) and a second instruction (the instruction <branch to GetLock if lock available> in line 2, see col. 6, line 57), the first instruction having an implicit operand from a predetermined register (event identification register 103, see Figs. 2 and 7) indicating a monitor address (lock address 139 in memory 137, see Fig. 2); execution resources (thread processing units TPU #1 to TPU #N see Fig. 2) to execute the first instruction and the second instruction (the instruction <branch to GetLock if lock available> in line 2,

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see col. 6, line 57) and to enter a first implementation dependent state (when an "armed" watch flag indication 105 is set, see Co. 5, lines 58-60) in response to the second instruction if the first instruction has been executed and no break events (break events such as a change to the lock 139 referenced in the event identification register 103) have occurred after execution of the first instruction; a monitor (event monitor 109, see Fig. 2) to cause exit from the first implementation dependent state in response to a memory access (see Col. 6, lines 1-6, regarding a change to the lock 139 referenced in the event identification register 103) to the monitor address.

As to claim 71, Emer et al.'741 also discloses: the processor of claim 70 wherein said monitor is to cause resumption of the first thread in response to events that cause a translation look-aside buffer to be flushed (since Emer et al.'741's system certainly uses a virtual addresses using "virtual" registers, and mapper 361, see Fig. 4, is best reasonably and broadly interpreted as a translation look-aside buffer see Col. 6, lines 40-49).

As to claim 72, Emer et al.'741 also discloses: the processor of claim 70 wherein said monitor is to cause

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resumption of the first thread in response to a write to a control register CRO (see Col. 5, lines 39-40, regarding the write to a specified location in memory space and this the situation the location is a control register).

As to claim 73, Emer et al.'741 also discloses: the processor of claim 72 wherein said monitor is to cause resumption of the first thread in response to an interrupt or a fault (see Col. 5, lines 39-40, regarding the write to a specified location in memory space and note the write will eventually cause an interrupt for the I/O operation).

As to claims 74 and 75, Emer et al.'741 also discloses: as best understood, said suspend logic (as set forth this is certainly inside the Emer et al.'741's system, such as a control unit comprising Quiesce Logic 110 see Fig. 2) is only to suspend said first thread if said monitor address (Lock 139, see fig. 2) is a selected memory type (the address type in memory 137, see Fig. 2).

As to claim 76, Emer et al.'741 also discloses: the processor of claim 74 wherein said selected memory type is a write-back type of memory (since the memory 137 will be updated eventually).

As to claim 78, Emer et al.'741 also discloses: the processor wherein a powerdown event is not a monitor break event (since



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the Emer et al.'741 does not indicate to use the powerdown event for controlling the system).

As to claim 79, Emer et al.'741 also discloses: the processor of claim 70 further comprising an instruction buffer (355 see Fig. 4, and col. 6, lines 35-39) which can be combined to form a single partition dedicated to one thread or can be partitioned to be used by the plurality of threads (see col. 6, lines 35-39).

As to claim 80, Emer et al.'741 also discloses: the processor of claim 70 further comprising a front end (comprising fetch thread chooser 301, see Fig. 3 or map thread chooser 351, see Fig. 4), which performs microoperation (uOP) generation, generating uOPs from macroinstructions (since the fetched instructions will be decoded before execution in the Emer et al.'741's system).

As to claim 81, Emer et al.'741 also discloses: the processor of claim 80 wherein said processor is capable of out-of-order execution and wherein said first instruction is followed by a store fence (this is the step when using cache-coherence protocol as indicated in col. 7, lines 51-64).

As to claim 82, Emer et al.'741 also discloses: The processor of claim 70 wherein a second operand (in the instruction such as LDQ ARM R1, (R5), see Col. 6, line 56) specifies events to mask.

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As to claim 83, Emer et al.'741 also discloses: the processor of claim 82 wherein one mask bit (such as the bit in Watch flag 105) indicates that masked interrupts break restart the first thread (see Col. 6, lines 1-6, regarding a change to the lock 139 referenced in the event identification register 103) despite interrupts being masked.

As to claim 84, Emer et al.'741 also discloses: The processor of claim 70 wherein said first instruction is an instruction having only implicit operands (in the instruction such as LDQ ARM R1, (R5), see Col. 6, line 56).

As to claim 85, Emer et al.'741 also discloses: the processor of claim 70 further comprising: coherency logic (since the Emer et al.'741's system use cache-coherence protocol as indicated in col. 7, lines 51-64) to perform a read line transaction in conjunction with suspending the first thread.

As to claim 86, Emer et al.'741 also discloses: The processor of claim 85 wherein said coherency logic is to perform a cache line flush to flush internal caches in conjunction (since the invalid cache data will be updated in the cache therein) with suspending the first thread.

As to claim 87, Emer et al.'741 also discloses: The processor of claim 70 wherein said processor is to monitor for a request for ownership or an invalidate cycle to the monitor address

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(since the Emer et al.'741's system use cache-coherence protocol as indicated in col. 7, lines 51-64).

As to claim 88, Emer et al.'741 also discloses: The processor of claim 70 wherein said processor is to assert a hit signal during a snoop phase of a bus transaction implicating the monitor address (as set forth above since the Emer et al.'741's system use cache-coherence protocol as indicated in col. 7, lines 51-64).

As to claim 89, Emer et al.'741 also discloses: The processor of claim 88 wherein the monitor is to cause said plurality of partitionable resources (such as the thread processing units TPU #1 to TPU #N see Fig. 2) to be re-partitioned to accommodate execution of said first thread in response to the memory access to the monitor address.

As to claim 90, Emer et al.'741 also discloses: The processor of claim 89 wherein said plurality of partitionable resources (the thread processing units TPU #1 to TPU #N see Figs. 2 and 6) comprise: an instruction queue (such as 305 see Fig. 2); a re-order buffer (such as 361 see Fig. 2); a pool of registers (such as 309 see Fig. 2); a plurality of store buffers (such as 403A see Fig. 6).

As to claim 91, Emer et al.'741 also discloses: The processor of claim 90 further comprising: a plurality of

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duplicated resources (the thread processing units TPU #1 to TPU #N see Figs. 2 and 6), said plurality of duplicated resources being duplicated for each of said plurality of threads, said plurality of duplicated resources (the thread processing units TPU #1 to TPU #N see Figs. 2 and 6) comprising:

a plurality of processor state variables; an instruction pointer; register renaming logic (the above elements are certainly existing in the SMT system such as Emer et al.'741's processor shown in Figs. 2 and 6).

As to claim 92, Emer et al.'741 also discloses: The processor of claim 91 further comprising: a plurality of shared resources (the thread processing units TPU #1 to TPU #N see Figs. 2 and 6), said plurality of shared resources being available for use by any of said plurality of threads, said plurality of shared resources comprising: said plurality of execution units (such as ALUs inside the thread processing units TPU #1 to TPU #N see Figs. 2 and 6); a cache (311 see Fig. 3); a scheduler (such as controllers inside the thread processing units TPU #1 to TPU #N see Figs. 2 and 6).

As to claim 94, Emer et al.'741 also discloses: The processor of claim 93 wherein said implicit operand is to indicate a linear address, and wherein said processor further comprises address translation logic (such as mapper 361, see

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Fig. 4 and Col. 6, lines 40-49) to translate said linear address to obtain the monitor address which is a physical address.

As to claim 95, Emer et al.'741 also discloses: The processor of claim 93 further comprising: coherency logic (since the Emer et al.'741's system use cache-coherence protocol as indicated in col. 7, lines 51-64) to ensure that no cache in another processor coupled to the processor stores information at said monitor address in a modified or exclusive state (see Col. 7, lines 45-65 regarding "SHARED" and "Exclusive" states).

As to claim 96, Emer et al.'741 also discloses: The processor of claim 93 wherein said coherency logic is to assert a hit signal

in response to another processor snooping the monitor address (since the Emer et al.'741's system use cache-coherence protocol as indicated in col. 7, lines 51-64; and many CPUs are used in the system as shown in Fig. 6).

As to claim 97, Emer et al.'741 also discloses: The processor of claim 95 wherein said coherency logic is to assert a hit signal in response to another processor snooping the monitor address (as set forth above, since the Emer et al.'741's system use cache-coherence protocol as indicated in col. 7, lines 51-64; and many CPUs are used in the system as shown in Fig. 6).

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***Allowable Subject Matter***

6. Claims 98-115 are allowed. Please refer to the Office Action mailed 07/28/05 which sets forth the reasons for allowance.

***Response to Arguments***

7. Applicant's arguments mailed 12/01/05 have been considered but are moot in view of the new explanation and new ground(s) of rejection. As set forth in the art rejections above, Emer et al.'741 teaches the claimed invention.

Regarding the drawings and the 35 U.S.C. §112, second paragraph problems, Applicant's response has not completely overcome these objections and rejections.


***Contact Information***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful,

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the examiner supervisor, Kim Huynh, can be reached on (571) 272-4147. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

9. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 571-273-8300.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.



HENRY W. H. TSAI  
PRIMARY EXAMINER

February 20, 2006